Optimization of thin film silicon solar cells on highly textured substrates

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Doped layers made of nanostructured silicon phases embedded in a silicon oxide matrix were implemented in thin film silicon solar cells. Their combination with optimized deposition processes for the silicon intrinsic layers is shown to allow for an increased resilience of the cell design to the substrate texture, with high electrical properties conserved on rough substrates. The presented optimizations thus permit turning the efficient light trapping provided by highly textured front electrodes into increased cell efficiencies, as reported for single junction cells and for amorphous silicon (a-Si)/microcrystalline silicon (mc-Si:H) tandem cells. Initial and stabilized efficiencies of 12.7 and 11.3%, respectively, are reported for such tandem configuration implementing a 1.1 μm thick microcrystalline silicon bottom cell.

1 Introduction  Photovoltaics will increasingly contribute to the global energy mix in the future, requiring very large scale development and reduction of manufacturing costs. Thin film silicon is a promising technology in this context, as its deposition processes (principally plasma enhanced chemical vapour deposition, PECVD) are compatible with mass-production on large-area substrates, allowing for immediate costs reduction, as demonstrated in Ref. [1] with reported potential production costs of 0.5 Euros/Wp. Moreover, this technology combines availability and environmental sustainability of the main raw materials (silicon and hydrogen). The remaining technology constraint which has hindered a larger market share up to now is the limited conversion efficiency. Maximum stabilized efficiencies of 10% could be achieved for the best modules making use of the monolithic tandem interconnection of an hydrogenated amorphous silicon (a-Si:H) junction with a microcrystalline silicon (μc-Si:H) junction [1, 2].

In order to increase the efficiency of thin film silicon solar cells and modules, light scattering at textured interfaces is crucial [3–5]. This allows using thinner absorber layers in the a-Si:H solar cell, reducing the impact of light-induced metastable defects on the cell performance. In μc-Si:H junctions it can, to some extent, compensate the material lower absorption. Light scattering is typically achieved with textured substrate and/or electrode that precede the silicon deposition [4–9]. In the superstrate configuration, textured transparent conductive oxides (TCO) such as SnO2 [6], sputtered ZnO followed by a wet-etching [7, 8] and ZnO processed by low-pressure chemical vapour deposition [9] (LPCVD) are widely used as front electrodes. However, a limitation of the technology comes from the difficulty to grow thin film silicon solar cells with good and spatially...
uniform electrical performance on substrates with a high light trapping potential. The use of highly textured substrates, the non-fully conformal deposition of the thin films and the growth dynamics can result in the creation of undesired local current drains, degrading the electrical performance ($V_{OC}$ and/or fill factor, FF) and the reliability of the solar cells [10–14]. Benefits of the texture on efficiency can thus be partly or even completely lost. The optimization of the trade-off between electrical and optical cell performances is thus essential for any efficiency increase in thin film silicon solar cells. The TCO morphology can be adapted [11, 12] or its roughness limited to a certain extent [13, 14] to allow for an optimal silicon growth and ensure high electrical performance; however this is realized at the price of reduced light trapping capabilities. We show that the electrical performances of cells on highly textured substrates can also be improved by the use of doped silicon rich silicon oxide layers and by the optimization of the PECVD processes for the intrinsic materials growth. The demonstrated higher resilience of the cell design to the substrate texture is therefore of high interest to realize a more efficient light trapping while maintaining optimum electrical properties, and thus consecutively to improve thin film silicon solar cells efficiency.

We report on the performance of a-Si:H and μc-Si:H single junctions, and of a-Si:H/μc-Si:H tandem junctions deposited on LPCVD ZnO. The a-Si:H and the μc-Si:H junctions presented in these studies were, respectively, deposited in a small size version (30 × 40 cm$^2$) and in a medium size version (40 × 50 cm$^2$) of industrial KAI PECVD reactors. The presented developments are thus compatible with mass production.

2 Optimized processes and cell design for thin film silicon single junctions

Doped nanostructured silicon rich silicon oxide layers were integrated in a-Si:H and in μc-Si:H solar cell devices. These layers were synthesized by PECVD from a gas mixture of silane (SiH$_4$), hydrogen, phosphine (PH$_3$) or tri-methyl boron (B(CH$_3$)$_3$), respectively, for n-type and p-type doping, and of an oxygen precursor (CO$_2$ in this study). Characterization was performed on 100 nm thick layers deposited on glass: refractive index was retrieved from fitting spectroscopic ellipsometry measurements to a Tauc–Lorentz dispersion model, while co-planar dark conductivity ($\sigma$) was measured after annealing via two aluminium contacts evaporated on the sample surface. Optimization of the PECVD processes permitted a clear phase separation in the developed layers, with silicon rich clusters embedded in a silicon oxide matrix [15]. For the prepared mixed-phase material, a high n-type doping ratio PH$_3$/(PH$_3$ + SiH$_4$) of up to 5% could be realized without impacting the crystalline volume fraction or the nanostructure of the silicon rich phase. For such n-type films, refractive index and dark conductivity are reported in Fig. 1 for an increasing CO$_2$/SiH$_4$ gas flux ratio, and are thus shown to decrease for increasing oxygen content in the film. Layers with a refractive index down to 1.7 at 600 nm wavelength were successfully implemented in cells. While they exhibit a low co-planar dark conductivity of $10^{-5}$–$10^{-7}$ S/cm, their integration in the solar cell does not impact the electrical performance through an additional series resistance, thus indicating a transverse conductivity higher than $10^{-5}$ S/cm. This anisotropy in conduction with a preferred conduction in the growth direction of the film is an interesting property of these nanostructured silicon rich silicon oxide materials (referred to as nc-SiO$_x$:H in the following).

For p-type doping of the developed silicon rich silicon oxide materials, optical and electrical performances are detailed in Ref. [15]. The p-type doping ratio B(CH$_3$)$_3$/ (B(CH$_3$)$_3$ + SiH$_4$) is here limited to about 0.5%. A higher B(CH$_3$)$_3$ concentration is then shown to affect the crystalline volume fraction of the Si phase [15], consecutively reducing the layer conductivity [15]. In comparison to n-type doping, p-type layers with a minimum refractive index of about 2.5 can therefore be developed with sufficient transverse conductivity to be integrated in cell. For use as intermediate reflective layer (IRL) in a-Si:H/μc-Si:H tandem cells, n-type doping is therefore preferred because of the lower achievable refractive index. For both doping types and both a-Si:H and μc-Si:H junctions, the optimum oxide layers integrated in the cells detailed in the following correspond to layers with a maximum oxygen content (i.e. maximum CO$_2$/SiH$_4$ gas flux ratio) while keeping a sufficient transverse conductivity to not impact the cell electrical performance.

2.1 a-Si:H single junction

a-Si:H p-i-n cells with a thickness of 250 nm were deposited on 2 μm thick LPCVD ZnO front contacts, using a 2 μm thick LPCVD ZnO back contact and white-paint back reflector. For each substrate 16 cells were patterned to an active area of 0.25 cm$^2$ by lift-off and plasma dry-etching. All cells were deposited using a similar p-layer stack, and were characterized through current–voltage measurements under a 1 sun illumination.
at standard test conditions. The corresponding open circuit voltage ($V_{OC}$), FF, short-circuit current density ($J_{SC}$) and conversion efficiency ($\eta$) are reported in Fig. 2 for each front contact type. For each substrate the best cell value is reported together with the mean value averaged out of the ten best cells. The TCO layers were either used as-grown (Z2) or lightly and heavily treated (Z2+ and Z2++), for a standard design and an optimized design with an n-type silicon oxide interlayer and improved i-layer.

The as-grown Z2 TCO thus yields the highest short circuit current density ($J_{SC}$) with a relative increase of 7.2% compared to the smoother Z2++. However, the electrical performances of cells using a standard n-type µc-Si:H are reduced for the as-grown ZnO, and are optimum for the heavily treated front electrode. A relative loss in $V_{OC} \times$ FF of up to 10% is observed between the Z2++ and Z2 electrodes (Fig. 2). The optical gain with the rougher substrate is therefore lost in this case and the optimum efficiency is realized with the Z2++ electrode.

A n-type nc-SiO$_2$:H resistive interlayer was then implemented in the cell design, as detailed in Ref. [16]: it was integrated in between a thin n-type µc-Si:H layer acting as a seed layer and a second n-type µc-Si:H layer ensuring a good contact to the back ZnO. The combined integration of this nc-SiO$_2$:H interlayer and of an i-layer deposited at 1.6 Å/s (instead of a deposition rate of 3 Å/s in the standard design), is shown to allow retaining high electrical properties on the rougher substrates (see Fig. 2). A drop in $V_{OC} \times$ FF of only 2% is realized when going from the smooth to the rough substrates with the optimized cell design. Regarding the optical performance, a slight current loss is observed for all substrate types in the proposed configuration. The n-layer stack transparency was not fully optimized in this study, and the losses can be attributed to increased parasitic absorption losses in the additional nc-SiO$_2$:H and n-type µc-Si:H layers added to the standard design. For the as-grown TCO layer and in comparison to cells deposited following the standard design, an efficiency gain of about 4% is realized with the use of the n-type nc-SiO$_2$:H interlayer [16], as also reported in Ref. [17], while an efficiency gain of 6% is realized with the combination of this interlayer with an i-layer deposited at 1.6 Å/s (Fig. 2). This demonstrates that both cell design techniques (introduction of an oxide interlayer) and PECVD process optimization for the i-layer can result in an increased resilience of the cell performance to the substrate roughness. In our study, the combination of both optimizations therefore permits using the efficient light trapping provided by the Z2 substrate to realize the highest initial cell efficiency in this series, above 11%, with no anti-reflective coating applied neither to the air/glass nor to the glass/TCO interfaces. It must be further noted that similar trends are kept after light induced degradation of the solar cells.

### 2.2 µc-Si:H single junction

The growth dynamics of µc-Si:H onto substrates exhibiting pyramidal features with high angles and/or low curvature radii in the bottom of the V-shaped valleys were already shown to possibly result in the creation of local nanoporous material regions [9–14]. These low-quality material regions were shown to result into decreased electrical properties of the solar cells because of an increased reverse saturation current ($J_0$) [12, 13]. To recover reasonable electrical properties, different approaches are presented so as to reduce the density or the impact of these local current drains. First of all, the plasma treatment of rough ZnO layers permits to turn V-shaped valleys into U-shaped valleys, decreasing the density of local current drains and resulting into a decreased $J_0$ [11, 12]. The cells presented in this study were thus deposited on 4.5 µm thick ZnO layers subjected to light (Z5+) and heavy (Z5+++) plasma treatments. Then, the deposition process conditions can also be adapted to minimize the performance drop, and a ‘process 1’ i-layer deposited at 0.3 nm/s was therefore compared to a ‘process 2’ i-layer deposited at 1 nm/s. Finally the impact of the incorporation of nc-SiO$_2$:H p-type [15] and n-type layers instead of the standard µc-Si:H doped layers was studied. Single junction µc-Si:H cells with i-layer thicknesses of 1.6 µm were deposited on each front electrode type (Z5+ and Z5+++), with both i-layer processes, and using standard
doped layers or the nc-SiO\textsubscript{x}H doped layers. All intrinsic layers deposited in this study have a crystalline volume fraction between 60 and 70\%. The cells were patterned by lift-off and plasma dry-etching to an active surface of 0.25 cm\textsuperscript{2}. Performances attained with the different combinations are summarized in Table 1.

The plasma treatment of the front electrode results in increased electrical properties in all cases. However, the average \(J_{\text{SC}}\) measured out of all the cells is reduced from 25.2 mA/cm\textsuperscript{2} for the Z5\textsuperscript{+} to 23.6 mA/cm\textsuperscript{2} for the Z5\textsuperscript{++} substrate. The i-layer process 2 is then shown to yield electrical properties more sensitive to the TCO roughness than the i-layer process 1. While an adapted morphology of the front TCO (as realized by the Z5\textsuperscript{++} substrate with U-shaped valleys) combined with an optimum i-layer process are confirmed to decrease the undesired current drains in the solar cell, the implementations of nc-SiO\textsubscript{x}H doped layers in the cell design are also shown to improve the electrical properties of the cells, leading in all cases to higher efficiencies, as reported in Table 1. A maximum relative efficiency gain of 30\% with the use of p-type and n-type nc-SiO\textsubscript{x}H doped is even realized for the cells grown on the rougher electrode using the most sensitive i-layer process.

For the a-Si:H and the μc-Si:H junctions, it can therefore be noted that both an improved cell design with the incorporation of doped silicon rich silicon oxide layers and an optimization of the PECVD process for the i-layer growth can result into an increased resilience of the electrical performance to the substrate roughness. The gain observed with the doped silicon oxide layers scales with the substrate roughness and with the i-layer process sensitivity to the substrate roughness. These results suggest that the oxide layers mitigate the impact of the local defective parts on the global cell performance. To take into account the thin film silicon solar cell non-uniformities, the cell can be regarded as a random diode array [18–20] consisting in a parallel combination of random ‘good’ diodes and of weak (low \(V_{\text{OC}}\)) diodes which can be operated in forward bias, shunting the system and resulting in an increased cell \(J_0\), as observed in Ref. [12]. The doped oxide layers act as a distributed resistance between these cell parts and the contact. The anisotropic nature of the layers can improve the separation between the active cell elements and the spatially localized current leaks. For high current drains localized into small areas, the voltage drop at the oxide layer can be locally high so that the effective potential driving these weak diodes and shunts can be lower than the operating voltage of the active cell parts. The current drains in the cell could thus be quenched by the use of the oxide layers, resulting in reduced impact of the low-quality regions onto the overall cell \(V_{\text{OC}}\) and FF. The proposed effects are consistent with the observed optimum resistivity of the oxide layers [17], for which the quenching of current leaks leads to a larger gain in performance than the losses relative to the increased cell series resistance. The presented explanations are also consistent with the observed maximum effect for cells on the rougher substrates and for the most sensitive i-layer processes, for which a higher density of local current drains can be expected. Finally, the cell regions with increased porosity are also vulnerable to in-diffusion of air and contaminants, which can degrade cell electrical performance. The amorphous O-rich matrix of the implemented SiO\textsubscript{x} films could also be possibly here acting as a barrier reducing the in-diffusion of water-vapour and possibly contaminants.

Regarding the two different μc-Si:H i-layer processes, further studies are on-going to gain an in-depth understanding of the differences in the quality of the bulk material and of the grain boundaries passivation. These studies will aim to understand how to relate the material bulk and passivation quality and the plasma processes parameters to the increased resilience to the substrate roughness.

In the present studies, the nc-SiO\textsubscript{x}H doped layers are shown to reduce current drains, but they cannot neither block them nor inhibit carriers recombination at the low-quality material regions. A reduction of the local current drains density is thus still crucial to realize an optimum device. In our studies, only the combination of the optimum i-layer process with the doped silicon oxide layers permit to convert the efficient light trapping of the Z5\textsuperscript{+} substrate into a high efficiency of 9.5\% (see Table 1), here again realized without using any anti-reflective coatings applied to the air-side of the front glass nor to the glass/TCO interface.

### Table 1 Performance of 1.6 μm thick μc-Si:H cells deposited on a rough (Z5\textsuperscript{+}) and smooth (Z5\textsuperscript{++}) substrate, with two i-layer processes realized in the same PECVD reactor, and using standard or oxide based doped layers.

<table>
<thead>
<tr>
<th>cell description</th>
<th>(J_{\text{SC}}) (mA/cm\textsuperscript{2})</th>
<th>(V_{\text{OC}}) (mV)</th>
<th>FF (%)</th>
<th>efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Z5\textsuperscript{+}, i-layer 2, std design</td>
<td>24.5</td>
<td>484</td>
<td>66</td>
<td>7.8</td>
</tr>
<tr>
<td>SiO-design</td>
<td>23</td>
<td>512</td>
<td>70</td>
<td>8.25</td>
</tr>
<tr>
<td>Z5\textsuperscript{+}, i-layer 2, std design</td>
<td>25.5</td>
<td>416</td>
<td>59</td>
<td>6.3</td>
</tr>
<tr>
<td>SiO-design</td>
<td>24</td>
<td>510</td>
<td>67</td>
<td>8.2</td>
</tr>
<tr>
<td>Z5\textsuperscript{++}, i-layer 1, std design</td>
<td>23.8</td>
<td>518</td>
<td>72</td>
<td>8.9</td>
</tr>
<tr>
<td>SiO-design</td>
<td>23.65</td>
<td>525</td>
<td>73</td>
<td>9.05</td>
</tr>
<tr>
<td>Z5\textsuperscript{+}, i-layer 1, std design</td>
<td>25.5</td>
<td>500</td>
<td>70</td>
<td>8.9</td>
</tr>
<tr>
<td>SiO-design</td>
<td>25.4</td>
<td>520</td>
<td>72</td>
<td>9.5</td>
</tr>
</tbody>
</table>

3 High efficiency a-Si:H/μc-Si:H tandem solar cells

Results discussed in Section 2 for a-Si:H and μc-Si:H cells show that after optimizations of the cell design and of
the i-layer processes, good electrical properties can be maintained on highly textured substrates. The developed nc-SiO\textsubscript{x}:H doped layers and the optimized i-layer processes were therefore used to develop a-Si:H/\textmu c-Si:H tandem cells on a LPCVD ZnO optimized for efficient light trapping. This front contact solution, derived from the studies presented in Ref. [21], is highly transparent and was only slightly treated. It thus still exhibits sharp pyramidal features, as it can be seen from the scanning electron microscope (SEM) image taken after a focus ion beam (FIB) cut of the developed a-Si:H/\textmu c-Si:H tandem cell (see Fig. 3).

The developed cells were patterned with an active area of 1.2 cm\textsuperscript{2}. They integrate a 260 nm thick a-Si:H top cell, which makes use of a 30 nm thick n-type nc-SiO\textsubscript{x}:H interlayer, and of an i-layer deposited at 1.6 A/\textmu s. The silicon oxide interlayer, seen in Fig. 3 thanks to a darker contrast than the top and bottom cells, is both acting as an intermediate reflector and as a resistive interlayer. Finally, the \textmu c-Si:H bottom cell is 1.1 \mu m thick and makes use of both p-type [15] and n-type nc-SiO\textsubscript{x}:H, and of the optimum i-layer process 1 as presented in Section 2. The tandem cell structure is illustrated in the inset of Fig. 3.

The implemented front electrode leads to an efficient light trapping in the tandem cell, as a summed current density of 25.7 mA/cm\textsuperscript{2} is realized with a bottom cell thickness of only 1.1 \mu m. Initial $J_{SC}$ of 13.2 and 12.5 mA/cm\textsuperscript{2} are attained in the a-Si:H and in the \textmu c-Si:H cells, respectively (see Fig. 4), using an anti-reflective coating on the air-side of the glass.

The optimized cell designs and i-layer processes permit to retain high electrical performances in the initial state ($V_{OC} = 1.36$ V, FF = 74.5%, see Fig. 5), even for the rough front electrode used. More importantly, these high electrical properties are conserved in the stabilized state ($V_{OC} = 1.345$ V, FF = 68.5%, see Fig. 5), i.e. after 1000 h of light induced degradation (LID) at 50 °C under a 1 sun equivalent illumination. This demonstrates that the implemented optimizations combined with efficient light trapping scheme result in thin film silicon solar cells with a high stabilized efficiency. After a relative LID of 12.5%, an a-Si:H/\textmu c-Si:H tandem cell with a \textmu c-Si:H cell thickness of about 1.1 \mu m (see Fig. 3) and with a stabilized efficiency of 11.3% is therefore reported (see Fig. 5). A close stable efficiency was realized in the past in our laboratory with 11.1% achieved without using any anti-reflective layer applied on the air-side of the glass (estimated at a possible 11.3–11.4% using an ARC). However, this was realized by
using much thicker layers with a 300 nm a-Si:H cell, a 150 nm thick intermediate reflector and a 3 μm thick μc-Si:H cell [9].

4 Conclusions The presented optimizations of the a-Si:H and μc-Si:H cell designs and processes were shown to result in improved electrical properties for cells deposited on textured front electrode. A high stabilized efficiency of 11.3% was reported for a tandem cell with a bottom cell thickness of 1.1 μm. Such high stable efficiency realized using a relatively thin μc-Si:H absorber material (~1 μm) shows that this approach has a high potential for lowering thin film silicon technologies production costs. The optimizations presented are moreover of high interest for further increasing thin film silicon solar cell efficiencies, as a cell design with an increased robustness to the substrate texture is demonstrated. This will certainly lead to an improved integration of nanophotonic structures optimized for advanced light trapping into functional high performance solar cell devices.

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